Deliverable FI3-D1.5.4
Click-to-Hardware Compiler

Teemu Rinta-aho, Mika Karlstedt

Tivit Future Internet Program
(Tivit FI)

Period: 1.4.2011 – 30.9.2011

Tivit, Strategisen huippuosaamisen keskittymän tutkimusohjelma

Rahoituspäätös 1171/10, 30.12.2010, Dnro 2790/31/2010

www.futureinternet.fi

www.tivit.fi

This work was supported by TEKES as part of the Future Internet programme of TIVIT (Finnish Strategic Centre for Science, Technology and Innovation in the field of ICT).

Executive summary / Internal release

Title:

Click-2-NetFPGA toolchain – a toolchain that can compile a Click software router to a hardware design loadable into a NetFPGA card.

Content: A compiler toolchain running on Linux computers and a scientific publication submitted to the USENIX ATC '12 conference.

Impact: Showing that it is possible to compile existing software router to hardware. Previous attempts have restricted the used set of the source programming language. In this activity, we have shown that it is possible to allow the programmer to use unrestricted C++ and that can still be transformed into hardware. This allows for faster prototyping of hardware routers in future research and these techniques may also be used to fasten product development.

Contact info: Teemu Rinta-aho <teemu.rinta-aho@ericsson.com>

Link: If the paper is published, it can be downloaded from the conference web site (http://static.usenix.org/events/atc12/index.html). Until then, access is restricted but a copy may be requested from the authors. On the next page there is a short summary of the work achieved. Once the paper is published, we can make all results fully public.

The toolchain software package is available to project partners upon request from the authors as well.

Introduction

High Level Synthesis (HLS) is a promising technology where algorithms described in high level languages are automatically transformed into a hardware design. Using HLS, a software developer can target reprogrammable chips such as FPGAs to enable fast prototyping with real hardware, or a direct implementation in the form of an ASIC. Although many HLS tools exist, they are mainly targeting developers who want to use a high level programming language to design hardware and usually support only a subset of the source language. Synthesizing existing software written in non-restricted C++ is so complicated that none of the current tools can handle that automatically.

In this deliverable, we have created a compiler toolchain that automatically transforms existing software in a limited domain to a functional hardware design. We have selected the Click Modular Router as the input system, and the Stanford NetFPGA as the target hardware platform. Our toolchain uses LLVM to transform Click C++ code into a form suitable for hardware implementation and then uses AHIR, a high level synthesis toolchain, to produce a VHDL netlist. The resulting netlist has been verified with actual hardware on the NetFPGA platform, and the results are encouraging. We foresee that the same principles could be applied to different domains, source languages and targets.

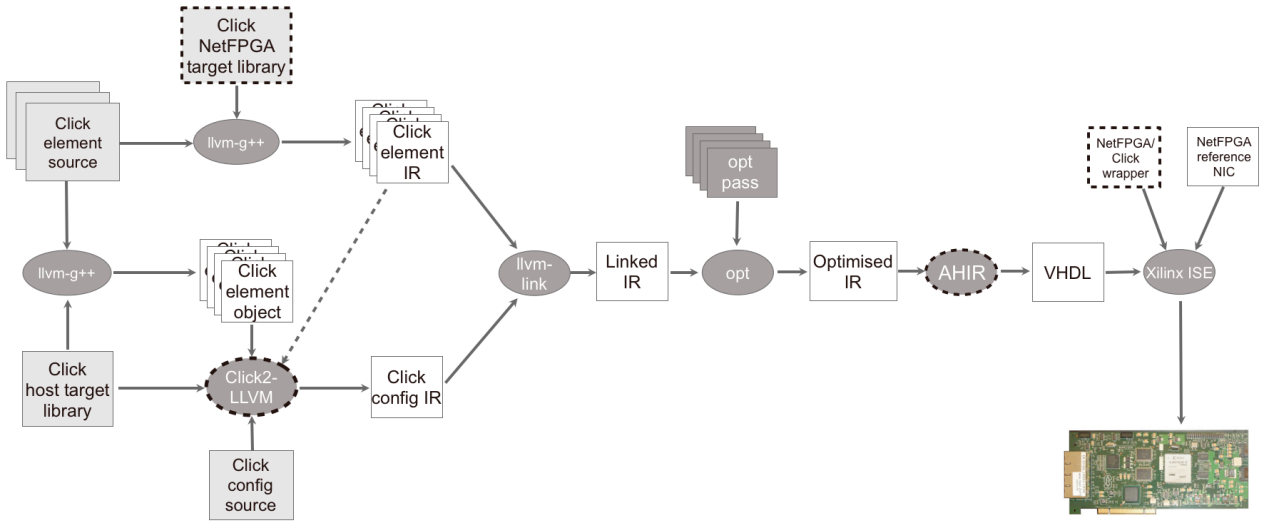

Figure 1: The Click2NetFPGA toolchain

The toolchain consists of four main components: LLVM, Click2LLVM, AHIR, and Xilinx ISE. The Click Modular Router is the source system for our compiler, and NetFPGA is the target. The main implementation efforts in the project have been in the the Click2LLVM and AHIR tools. Click2LLVM transforms a Click router configuration into a single LLVM module. AHIR transforms LLVM into VHDL. We have glued the operation of these different steps together with several Makefiles, scripts and integration efforts in different tools. Everything else except the Xilinx ISE is open source and can be further developed. Although we have chosen the Click and the NetFPGA, the ideas could be used elsewhere. The source language could be different, and the target could be e.g. ASIC.